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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,682	02/08/2002	Rob Lofland	CALIP008/P068	2522

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BEYER WEAVER & THOMAS LLP
P.O. BOX 778
BERKELEY, CA 94704-0778

EXAMINER	
WOOD, KEVIN S	

ART UNIT	PAPER NUMBER
2874	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,682	LOFLAND ET AL.	
	Examiner	Art Unit	
	Kevin S Wood	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,15-21,24,25,28-34,37,38 and 41-47* is/are rejected.

7)☒ Claim(s) *11-14,22,23,26,27,35,36,39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0202*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4, 15-18, 24, 28-31, 33, 37, 38, 41, 42, 44, and 46 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0041409 to Laham et al.

Referring to claims 1, 2, 4 and 15, Laham et al. discloses all the limitations of the claimed invention. Laham et al. discloses an optical switch testing system (OSTS) for testing an device under test (DUT), the DUT (2) including a plurality of optical input ports (201-208) and a plurality of optical output ports (211-218), the system including: at least one processor; memory; a plurality of OSTS output ports, wherein a selected plurality of the OSTS output ports are each optically connected to a respective DUT input port (201-208); a plurality of OSTS input ports, wherein a selected plurality of the OSTS input ports are each connected to a respective DUT output port (211-218); an optical test stimulation (20) component configured or designed to generate optical test signals to be transmitted to a selected plurality input ports of the DUT; and an optical

test detection component (33)configured or designed to detect a presence or absence of light on a selected plurality output ports of the DUT. See Fig. 1 through Fig. 4 of the reference, along with their respective portions of the specification. Laham et al. discloses that the DUT is a photonic optical cross-connect device (2).

Referring to claims 16-18, 24 and 28, Laham et al. discloses all the limitations of the claimed method. Laham et al. discloses a method for performing testing of an optical device under test (DUT), the DUT (2) including a plurality of DUT optical input ports (201-208) and a plurality of DUT optical output ports (211-218), the testing being performed by an optical switching testing system (OSTS), the OSTS including a plurality of OSTS output ports optically connected to a plurality of DUT input ports (201-208), the OSTS further including a plurality of OSTS input ports optically connected to a plurality of DUT output ports (211-218), the method including: configuring components (4,20,33) of the OSTS in order to perform a specific test on the DUT; configuring a first test scenario (103) at the DUT; transmitting at least one optical test signal (104) to at least one DUT output port; obtaining test results by monitoring (105) at least one DUT output port for the presence of absence of light; and analyzing the test results for specific characteristics. See Fig. 1 through Fig. 4 of the reference, along with their respective portions of the specification. Laham et al. also discloses automatically reconfiguring the DUT for a second test scenario; automatically implementing the specific test on the DUT; and obtaining test results associated with the second test scenario from the DUT.

Referring to claims 29, 31, 33, 37, 38 and 41, Laham et al. discloses all the limitations of the claimed invention. Laham et al. discloses an optical switch testing system (OSTS) for testing an device under test (DUT), the DUT (2) including a plurality of optical input ports (201-208) and a plurality of optical output ports (211-218), the system including: at least one processor; memory; a plurality of OSTS output ports, wherein a selected plurality of the OSTS output ports are each optically connected to a respective DUT input port (201-208); a plurality of OSTS input ports, wherein a selected plurality of the OSTS input ports are each connected to a respective DUT output port (211-218); an optical test stimulation (20) component configured or designed to generate optical test signals to be transmitted to a selected plurality input ports of the DUT; and an optical test detection component (33)configured or designed to detect a presence or absence of light on a selected plurality output ports of the DUT; the system being configured or designed to configure components of the OSTS in order to perform a specific test on the DUT; the system being further configured or designed to configure a first test scenario (background mode) at the DUT; the system being further configured or designed to transmit at least one optical test signal to at least one DUT input port; the system being further configured or designed to obtain test results by monitoring at least one DUT output port for the presence or absence of light; and the system being further configured or designed to analyze the test results for specific characteristics. See Fig. 1 through Fig. 4 of the reference, along with their respective portions of the specification.

Referring to claim 30, Laham et al. discloses all the limitations of the claimed invention. Laham et al. discloses the system being further configured or designed to

automatically reconfigure the DUT for a second test scenario (real time mode); the system being further configured or designed to automatically implement the specific test on the DUT; and the system being further configured or designed to obtain test results associated with the second test scenario from the DUT.

Referring to claims 42, 44, and 46, Laham et al. discloses all the limitations of the claimed invention. Laham et al. discloses an optical switch testing system (OSTS) for testing an device under test (DUT), the DUT (2) including a plurality of optical input ports (201-208) and a plurality of optical output ports (211-218), the system including: at least one processor; memory; a plurality of OSTS output ports, wherein a selected plurality of the OSTS output ports are each optically connected to a respective DUT input port (201-208); a plurality of OSTS input ports, wherein a selected plurality of the OSTS input ports are each connected to a respective DUT output port (211-218); an optical test stimulation (20) component configured or designed to generate optical test signals to be transmitted to a selected plurality input ports of the DUT; and an optical test detection component (33)configured or designed to detect a presence or absence of light on a selected plurality output ports of the DUT; means for configuring components of the OSTS in order to perform a specific test on the DUT; means for configuring a first test scenario (background mode) at the DUT; means for transmitting (21) at least one optical test signal to at least one DUT port; means for obtaining test results by monitoring at least one DUT output port for the presence or absence of light; and means for analyzing the test results . See Fig. 1 through Fig. 4 of the reference, along with their respective portions of the specification.

Referring to claim 43, Laham et al. discloses all the limitations of the claimed invention. Laham et al. discloses the system having means for automatically reconfiguring the DUT for a second test scenario (real time mode); means for automatically implementing the specific test on the DUT; and means for obtaining test results associated with the second test scenario from the DUT.

3. Claims 1, 3-10 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,590,644 to Coin et al.

Referring to claims 1, 3-10 and 15, Coin et al. discloses all the limitations of the claimed invention. Coin et al. discloses an testing system for testing an device under test (DUT), the DUT (110) including a plurality of optical input ports and a plurality of optical output ports, the system including: at least one processor (70); memory (230); a plurality of testing system output ports, wherein a selected plurality of the OSTS output ports are each optically connected to a respective DUT input port; a plurality of testing system input ports, wherein a selected plurality of the testing system input ports are each connected to a respective DUT output port; an optical test stimulation (6) component configured or designed to generate optical test signals to be transmitted to a selected plurality input ports of the DUT; and an optical test detection component (80,130,170) configured or designed to detect a presence or absence of light on a selected plurality output ports of the DUT. See Fig. 1 through Fig. 14 of the reference, along with their respective portions of the specification.

Referring to claims 16-21, 24 and 28, Coin et al. discloses all the limitations of the claimed method. Coin et al. discloses a method for performing testing of an optical device under test (DUT), the DUT (110) including a plurality of DUT optical input ports and a plurality of DUT optical output ports, the testing being performed by an optical testing system, the optical testing system including a plurality of optical testing system output ports optically connected to a plurality of DUT input ports, the optical testing system further including a plurality of optical testing system input ports optically connected to a plurality of DUT output ports, the method including: configuring components of the OSTS in order to perform a specific test on the DUT; configuring a first test scenario at the DUT; transmitting at least one optical test signal to at least one DUT output port; obtaining test results by monitoring at least one DUT output port for the presence of absence of light; and analyzing the test results for specific characteristics. See Fig. 1 through Fig. 14 of the reference, along with their respective portions of the specification.

Referring to claims 29-34, 37, 38 and 41, Coin et al. discloses all the limitations of the claimed invention. Coin et al. discloses an optical testing system for testing an device under test (DUT), the DUT (110) including a plurality of optical input ports and a plurality of optical output ports, the system including: at least one processor (70); memory (230); a plurality of optical testing system output ports, wherein a selected plurality of the optical testing system output ports are each optically connected to a respective DUT input port; a plurality of optical testing system input ports, wherein a selected plurality of the optical testing system input ports are each connected to a

respective DUT output port; an optical test stimulation (6) component configured or designed to generate optical test signals to be transmitted to a selected plurality input ports of the DUT; and an optical test detection component (80,130,170) configured or designed to detect a presence or absence of light on a selected plurality output ports of the DUT; the system being configured or designed to configure components of the OSTS in order to perform a specific test on the DUT; the system being further configured or designed to configure a first test scenario at the DUT; the system being further configured or designed to transmit at least one optical test signal to at least one DUT input port; the system being further configured or designed to obtain test results by monitoring at least one DUT output port for the presence or absence of light; and the system being further configured or designed to analyze the test results for specific characteristics. See Fig. 1 through Fig. 14 of the reference, along with their respective portions of the specification.

Referring to claims 42-47, Laham et al. discloses all the limitations of the claimed invention. Laham et al. discloses an optical testing system for testing an device under test (DUT), the DUT (110) including a plurality of optical input ports and a plurality of optical output ports, the system including: at least one processor (70); memory (230); a plurality of OSTS output ports, wherein a selected plurality of the optical testing system output ports are each optically connected to a respective DUT input port; a plurality of optical testing system input ports, wherein a selected plurality of the optical testing system input ports are each connected to a respective DUT output port; an optical test stimulation (6) component configured or designed to generate optical test signals to be

transmitted to a selected plurality input ports of the DUT; and an optical test detection component (80,130,170) configured or designed to detect a presence or absence of light on a selected plurality output ports of the DUT; means for configuring components of the optical testing system in order to perform a specific test on the DUT; means for configuring a first test scenario at the DUT; means for transmitting at least one optical test signal to at least one DUT port; means for obtaining test results by monitoring at least one DUT output port for the presence or absence of light; and means for analyzing the test results . See Fig. 1 through Fig. 14 of the reference, along with their respective portions of the specification.

Allowable Subject Matter

4. Claims 11-14, 22, 23, 26, 27, 35, 36, 39, and 40, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Referring to claim 11, the primary reason for this claim being allowable is the inclusion of the limitation wherein the plurality of demodulator circuits includes at least 8 separate demodulator circuits.

Referring to claim 12, the primary reason for this claim being allowable is the inclusion of the SONET traffic analyzer.

Referring to claim 13, the primary reason for this claim being allowable is the inclusion of a Gigabit Ethernet traffic analyzer.

Referring to claim 14, the primary reason for this claim being allowable is the inclusion of a polarization scrambler to scramble or randomize a state of polarization of test optical signals.

Referring to claims 22, 23, 35, and 36, the primary reason for this claim being allowable is the inclusion of automatic testing for optical cross-talk testing on a selected plurality of different optical paths.

Referring to claims 26 and 39, the primary reason for this claim being allowable is the inclusion of automatic testing for insertion loss on a selected plurality of different optical paths.

Referring to claims 27 and 40, the primary reason for this claim being allowable is the inclusion of automatic testing for path switching time on a selected plurality of different optical paths.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Application Publication No. 2003/0210850 to DeAngelis et al.

U.S. Patent Application Publication No. 2003/0044107 to Tamer et al.

U.S. Patent No. 6,574,384 to Cannell et al.

U.S. Patent No. 6,519,383 to Cannell et al.

U.S. Patent No. 6,456,751 to Bowers et al.

Each of these references discloses an optical switch testing system and method similar to that of the claimed method.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin S Wood whose telephone number is (571) 272-2364. The examiner can normally be reached on Monday-Thursday (7am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rodney B Bovernick can be reached on (571) 272-2344. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KSW

AKM ENAYET ULLAH
PRIMARY EXAMINER